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# IMPACT: an architectural framework for multiple-instruction-issue processors

PP Chang, SA Mahike, WY Chen, NJ Warter, ... - ACM SIGARCH Computer Architecture News, 1991 - portal.acm.org ... these code optimizations and code scheduling techniques has ... al., use non-trapping **instructions** in the ... code motion and optimization than a traditional approach ...

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### Global code motion/global value numbering

C Click - ACM SIGPLAN Notices, 1995 - portal.acm.org

... 2. Global Code Motion ... 3, Schedule (select basic blocks for) all instructions early, based on existing control and data depend- ence. ...

Cited by 98 - Related articles - BL Direct - All 4 versions

# 

M Lam - Proceedings of the ACM SIGPLAN 1988 conference on ..., 1988 - portal.acm.org ... to satisfy the union of the **scheduling** constraints of ... By omitting empty machine

instructions at code emission time ... all other forms of code motion around the ...

Cited by 1024 - Related articles - BL Direct - All 21 versions

#### Efficient instruction scheduling for a pipelined architecture- \*wisc.edu (PDF)

PB Gibbons, SS Muchnick - Proceedings of the 1986 SIGPLAN symposium on ..., 1986 - portal.acm.org ... perform one based on linear code sequences: the ... they tend to bring related instructions closer together. ... the extension of instruc- tion scheduling across basic ...

Cited by 213 - Related articles - BL Direct - All 12 versions

## Code scheduling and register allocation in large basic blocks

JR Goodman, WC Hsu - Proceedings of the 2nd international conference on ..., 1988 - portal.acm.org ... the same register for unrelated instructions (so called ... Section 3 describes a code scheduling method which combines two code motion techniques - one to ...

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### 

SA Mahlke, WY Chen, WH Wen-mei, BR Rau, ... - Proceedings of the fifth international conference on ..., 1992 - portal. acm.org

... using the restricted percolation scheduling model [8]. Thus, only instructions which the compiler can guarantee to never ... ulative code motion. ...

Cited by 116 - Related articles - BL Direct - All 7 versions

#### A VLIW architecture for a trace scheduling compiler- \* Winois adu (PDF)

RP Colwell, RP Nix, JJ O'Donnell, DB ... - IEEE Transactions on Computers, 1988 - doi.ieeecomputersociety.org ... COMPACTING COMPILATION Multiflow's trace **scheduling** compacting compiler ... are converted into highly parallel wide-**instruction**-word **code** is transparent to ...

Cited by 498 - Related articles - All 20 versions

### EPIC: Explicitly parallel instruction computing

MS Schlansker, BR Rau - Computer, 2000 - ieeexplore.ieee.org

... of aggres- sive, compile-time **code motion** that would be illegal in a conventional architecture. Static **scheduling** A MultiOp **instruction** specifies multiple ...

Cited by 167 - Related articles - BL Direct - All 5 versions

## Iterative modulo scheduling: An algorithm for software pipelining loops-

BR Rau - Proceedings of the 27th annual international ..., 1994 - portal.acm.org

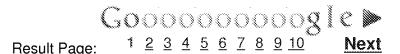
... software pipelining, the "move- then-schedule" approach, is to move instructions, one by ... Although such code motion can yield improvements in the schedule ...

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### Region scheduling: An approach for detecting and redistributing parallelism-

R Gupta, ML Soffa - IEEE Transactions on Software Engineering, 1990 - doi.ieeecomputersociety.org ... the data dependence subgraphs before **code** generation. ... transformation phase of region **scheduling** was implemented ... for a reconfigurable long **instruction** word (RLIW ...

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